

PRESS RELEASE**Comprehensive CPU Core and IP for Networking Seminar
Spotlights IP Integration and Design Techniques*****Program Includes EEMBC Presentation on Multicore Benchmark Strategy
and Next-Gen SoC Performance Testing***

MOUNTAIN VIEW, CA—March 6, 2008— The Linley Group, the leading provider of independent technology analysis for networking, communications, and consumer electronics semiconductors, today announced that its CPU Cores and IP for Networking seminar will be held in San Jose, California, on Wednesday, March 19, 2008. This one-day in-depth Linley Tech seminar will highlight leading-edge technology and include technical presentations that illustrate how CPU cores and IP for high-speed transceivers, security accelerators, and high-performance memory can be integrated into ASICs and SoCs. The seminar is free to qualified ASIC and SoC designers at chip suppliers and OEMs.

“Effectively integrating third-party CPU cores and supporting IP blocks is the key to successful implementation of complex system-on-chip (SoC) and ASIC (Application Specific Integrated Circuit) solutions,” said Linley Gwennap, president and principal analyst at The Linley Group. “We’ve selected our panel from leading industry experts to provide a day of informed insight for decision makers who are implementing or contemplating using advanced third-party IP.”

The Linley Group selects and screens speakers and presentations to ensure that the content is in-depth, application-focused, and relevant to the needs of the technical decision maker. Attendees will have a chance to meet, question, and interact with key industry participants from leading suppliers in the field and with The Linley Group analysts who cover the trends and technologies available in ASIC design.

Some of the highlights of the scheduled program include:

- **Linley Gwennap, Principal Analyst, The Linley Group**, will present "A CPU Cores and IP Overview"
- **Shay Gal-On, Director of Software Engineering, EEMBC**, will present "Analyzing Multicore and Networking Processor Performance"
- **Warren Savage, CEO, IPextreme**, will present "Licensing Freescale's Power Architecture and ColdFire Technologies"
- **Vidya Rajagopalan, Director of Engineering, MIPS**, will present "Accelerating Networking Functions Using MIPS32"
- **Harry Linzer, Senior Engineer, IBM**, will present "Building a Single-Chip Control/Data Plane"



- **Farid Nemati, CTO, T-RAM**, will present "Thyristor RAM: A Novel Embedded-Memory Technology"
- **Steve Singer, Systems Engineering Manager, SafeNet Systems**, will present "How Application Requirements Drive Security Architecture"
- **Jerry Redington, Principal System Architect, Tensilica**, will present "Networking Applications for Xtensa Configurable Processors"
- **Nandan Nayampally, Director of CPUs, ARM**, will present "Evaluating Multicore Tradeoffs for SMB Networking"
- **Navraj Nandra, Director of Product Marketing, Synopsys**, will present "Designing High-Speed Transceivers"

Location and Registration

The Linley Group CPU Cores and IP for Networking seminar will be held on Wednesday, March 19, 2008 at the DoubleTree Hotel in San Jose, California. The seminar is sponsored by Freescale, IBM, SafeNet, Tensilica, T-RAM, and EEMBC. For further information and online registration, visit:
http://www.linleygroup.com/Seminars/ip_cpu_cores.html

About The Linley Group

The Linley Group, the leading provider of independent technology analysis for networking, communications, and consumer electronics semiconductors, covers emerging areas such as high-speed embedded processors, Gigabit and 10G Ethernet, mobile communications processors, and more. The company provides in-depth technology reports and interactive seminars as well as strategic consulting services tailored to the individual client. To get free access to The Linley Group's analysis of recent news and events in these markets, subscribe to our e-mail newsletters. More information about The Linley Group is available at <http://www.linleygroup.com>.

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